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MARTINE PENILLA & GENCARELLA, LLP
710 LAKEWAY DRIVE
SUITE 200
SUNNYVALE, CA 94085

EXAMINER	
NGUYEN, HIEP	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/759,339	BECKER ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sh et with th correspond nce address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because the letters and numbers are not readable. A formal drawing is required. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 20-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 11 the recitation "a high drive pull-up transistor coupled to the second terminal of the p-channel transistor" on line 1 and 2 is indefinite because it is misdescriptive. Claim 11 depends upon claims 1 and 10. Claims 1 and 10 read on figure 4A of the present application. Figure 4A does not show the "a high drive pull-up transistor". Thus, claim 11 does not further limit claims 1 and 10.

Regarding claim 14, the recitation "increasing a voltage at an output of the inverting circuit in response to sensing the voltage transition change" on lines 2 and 3 is indefinite because it is not clear what is the "voltage transition change". The transition change could be at the input or output of the input buffer and the transition change can be from low to high or from high to low.

The recitation "increasing an impedance at a drain of an n-channel transistor in the inverting circuit in response to sensing the voltage transition change" is indefinite because it is not clear how the impedance can be increased at one "location" of a circuit, the drain of a transistor which is the output of the inverting circuit (406, 408).

Regarding claims 20 and 25, the recitation "an inverting circuit for transitioning a first voltage to a second voltage, the second voltage being **lower** than the first voltage" on lines 2 and 3 is indefinite because it is misdescriptive. If a **low** level (first voltage) is applied to the input of the "inverting circuit", the input signal is inverted and the output of the "inverting circuit" (the second voltage) must be **higher** that the first voltage instead of being **lower** than the first voltage as recited. The recitation "a circuit coupled to an output of the inverting circuit, the circuit initiating a voltage transition from a third voltage to the second voltage, the third voltage being lower than the second voltage before the inverting circuit initiates the voltage transition from the third voltage to the second voltage" on lines 3-6 is confusing. It is not clear what are the "a circuit", the "first voltage", "second voltage" and the "third voltage". Assume that the "a third voltage" is (COREVdd) and the "second voltage" at node (424) is a **low** voltage as recited on lines 2, 3 then the "third voltage" (COREVdd) cannot be **lower** than the second voltage as recited. The Applicant is requested to shows what are the "an inverting circuit", "a circuit", "a first voltage", "a second voltage" and "a third voltage" in the drawing and to explain why the "second voltage" is **lower** than the "first voltage" and the "third voltage" is **lower** than the second voltage. The same rationale is true for claim 25. The Applicant is requested to show in the drawing the "an inverting circuit", "a first predetermined voltage, " a second predetermined voltage" " a third predetermined voltage" and " a feed forward circuit".

Regarding claim 23, the recitation "the N-type transistor is coupled to the **output** of the inverting circuit and a **second terminal** of the N-type transistor is coupled to the **second**

voltage" on lines 2 and 3 is indefinite because it is misdescriptive. Figure 4A of the present application shows that the "circuit" (404) has a first terminal coupled to the output (424) of the "inverting circuit" and the second terminal coupled to the **supply voltage** (COREVdd). Note that as recited in claim 20, the "second voltage" is the voltage at the **output** of the "inverting circuit".

Claims 17-19, 21, 22 and 24 are indefinite because of the technical deficiencies of claims 14 and 20.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 9, 10 and 12-18 and 20-25 are rejected under 35 U.S.C. 102 (b) as being anticipated by Krishnamurthy (USP. 6,271,713).

Regarding claims 1-4, figure 5, of Krishnamurthy shows a feed forward circuit for reducing delay through an input buffer comprising:

an inverter having an input and an output (162);

an inverting circuit (164) having an input and an output, the input of the inverting circuit being coupled to the output of the inverter; and

a feed forward transistor (M1) having a gate coupled to the input of the inverter, and a terminal coupled to the output of the inverting circuit, wherein the feed forward transistor decreases an amount of time required for the output of the inverting circuit to change state (col.2 lines 50-64). Note that transistor (M1) pulls the output high before inverter (164) changes state. When the input to the inverter transitions to a HIGH state, transistor (M1) is turned on and the output is pulled to a high level. When the input to the inverter is LOW, transistor (M1) ceases to increase the voltage because it is turned off.

Regarding claim 5, the p-channel transistor of the inverting circuit is transistor (M4) and the n-channel transistor is transistor (M5).

Regarding claim 9, the feed forward transistor (M1) turns off, allowing the voltage at the output of the inverting circuit to transition to a LOW state when the input to the inverter transitions to a LOW state.

Regarding claim 10, the p-channel and the n-channel of the inverting circuit are transistors (M4) and (M5). The connections of these transistors are clearly shown in figure 5.

Regarding claims 12 and 13, figure 5 of Krishnamurthy shows a method for reducing delay through an input buffer comprising the operation off:

sensing a voltage transition change (via transistor M1) before a voltage at an input to an inverting circuit (164) changes state; and

changing a voltage at the output of the inverting circuit in response to sensing the voltage transition change (transistor M1 is turned on to pull the output voltage to a high level), wherein an amount of time required for the output of the inverting circuit to change state is decreased because transistor (M1) is turned on before inverter (164) changes state thus, the amount of time for the output of the inverting circuit to change state is decreased by a predetermined first time interval depending on the characteristics of the inverting circuit (164) and transistor (M1).

Regarding claims 14, 15 and 16, figure 5 of Krishnamurthy shows that when the input (Vin) changes from low to high, the n-channel transistor (M5) is turned off and thus, the impedance at the drain of the n-channel transistor (M5) increases. The output of the inverter (M2, M3) is coupled to the input of the inverting circuit (M4, M5). The feed forward transistor is the n-channel transistor (M1).

Regarding claims 17 and 18, the combination of the inverter (M1, M2) and the inverting circuit (M4, M5) provides a non-inverting buffer thus when the voltage at the input decreases, the voltage at the output of the inverting decreases.

Regarding claims 20, 21 and 22, figure 5 of Krishnamurthy shows "an inverting circuit" (162, 164). The "a circuit" is transistor (M1). Because of the propagation delay of inverter (164) transistor (M1) applies "a third voltage" on the output of the "inverting circuit" **before** the "inverting circuit" initiates a voltage transition. The input of the "inverting circuit" (104) is coupled to the "a circuit" (M1). Transistor (M1) is an n-type transistor.

Regarding claims 23 and 24, a first terminal of the N-type transistor (M1) is coupled to the output of the inverting circuit (162, 164) and a second terminal of the N-type transistor is coupled to the "second voltage" (Vdd). The gate of transistor (M1) is coupled to the input (104) of the inverting circuit.

Regarding claims 25, figure 5 of Krishnamurthy shows "an inverting circuit" (162, 164). The "a feed forward circuit" is transistor (M1). Because of the propagation delay of inverter (164), transistor (M1) applies "a third voltage" on the output of the "inverting circuit" **before** the "inverting circuit" initiates a voltage transition.

Claims 12-19 are rejected under 35 U.S.C. 102 (b) as being anticipated by Taylor (USP. 5,644,255).

Regarding claims 12 and 13, figure 4 of Taylor shows a method for reducing delay through an input buffer comprising the operation off:

sensing a voltage transition change (via transistor 204) before a voltage at an input to an inverting circuit (403, 404) changes state; and

changing a voltage at the output of the inverting circuit in response to sensing the voltage transition change (transistor 204 is turned on to pull the output voltage to a low level), wherein an amount of time required for the output of the inverting circuit to change state is decreased because transistor (204) is turned on before the inverting circuit (403, 404) changes state thus, the amount of time for the output of the inverting circuit to change state is decreased by a predetermined first time interval depending on the characteristics of the inverting circuit (403, 404) and transistor (204).

Regarding claims 14, 15 and 16, figure 4 of Taylor shows that when the input (Vin) changes from low to high, the n-channel transistor (403) is turned off and thus, the impedance at the drain of the n-channel transistor (403) increases. The output of the inverter (401) is coupled to the input of the inverting circuit (403, 404). The feed forward transistor is transistor (204).

Regarding claims 17, 18 and 19, the combination of the inverter (401) and the inverting circuit (403, 404) provides a non-inverting buffer thus when the voltage at the input decreases, the voltage at the output of the inverting decreases. The feed forward transistor (204) is a p-channel transistor.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy (USP. 6,271,713) in view of Schultz et al. (USP. 6,034,557).

Regarding claim 6, figure 5 of Krishnamurthy includes all the limitation of claim 6 except for the limitation that there is a high impedance transistor coupled to the second terminal of the n-channel transistor of the inverting circuit and having a terminal coupled to ground. Figure 1 of Schultz shows an inverting circuit having a high impedance transistor (N2) coupled to the n-channel transistor of the inverting circuit (N3, P3) to compensate for changes in transistor threshold voltages that affect all transistors occurring due to process variations (col. lines 40-51). Therefore, it would have been obvious to those skilled in the art to implement a high impedance transistor (N2) taught by Schultz to the n-channel transistor (M5) of the inverting circuit (M4, M5) of Krishnamurthy to compensate for changes in transistor threshold voltages that affect all transistors occurring due to process variations.

Claims 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy (USP. 6,271,713) in view Foss (USP. 4,786,830).

Regarding claims 7 and 8, figure 5 of Krishnamurthy includes all the limitation of claim 6 except for the limitation that there are a high and a low impedance transistors coupled between the n-channel of the inverting circuit and the ground. Figure 2 of Foss shows two transistors (6) and (9) coupled **in series** between the inverting circuit (20) and the supply terminal for avoiding a dc current path through inverter (20) (col. 4, lines 8-14). Therefore, it is old and well known in the art and would have been obvious to those having ordinary skill in the art to implement the transistors taught by Foss **in series** between the inverting circuit (M4,

M5) of Krishnamurthy and the **ground** for avoiding a dc current path through inverting circuit.

Regarding claim 8, figure 3 of Foss shows that the low impedance transistor (9) is off when the output of the inverting circuit is high, However, it is old and well known that a transistor is turned on by a low or high level control signal depending what type of transistor or the level of the control signal used. Because the combination of Krishnamurthy and Foss having the transistors coupled between the inverting circuit and the ground, it needs a low voltage to turn the low impedance transistor off.

Regarding claims 9 and 10, the feed forward transistor (M1) is turned off, the output of the inverting circuit is not connected to the supply voltage (Vdd) thus, the output of the inverting stays at a low level when the output of the inverting circuit transitions to a low state. The inverting circuit comprises an n-channel transistor (M5) and a p-channel transistor (M4) connected as shown in figure 5 of Krishnamurthy.

Regarding claim 11, figure 5 of Krishnamurthy includes all the limitation of claim 6 except for the limitation that the feed forward circuit further comprises a high drive pull-up transistor coupled to the p-channel and to a "core voltage". The high drive pull-up transistor is on when the output of the inverting circuit is low. Figure 2 of Foss show a high drive pull-up transistor (9) coupled to the inverting circuit (20) for avoiding a dc current path through inverter (20) (col. 4, lines 8-14). The high drive transistor (9) is turned on when the output of the inverting circuit is low. Therefore, it would have been obvious to those skilled in the art to implement a high drive pull-up transistor taught by Foss into the inverting circuit of Krishnamurthy (M4, M5) for avoiding a dc current path through inverter.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
01-07-04

TUAN T. LAM
PRIMARY EXAMINER